CLAIMS:

1. A method for extracting bit values from an incoming bit stream, the method comprising:

detecting transitions of the incoming bit stream;

for each transition of the incoming bit stream detected, determining a relative phase of the transition with respect to a reference clock signal;

determining an average relative phase of the detected transitions with respect to the reference clock signal;

based upon the average relative phase of the transitions with respect to the reference clock signal, determining a sampling phase with respect to the reference clock signal; and

sampling the incoming bit stream at the sampling phase with respect to the reference clock signal to extract the bit values.

2. The method of claim 1, wherein the incoming bit stream complies with the Universal Serial Bus 2.0 interface standard.

3. The method of claim 1, wherein determining an average relative phase of the detected transitions with respect to the reference clock signal comprises:

determining an initial average relative phase with respect to the reference clock signal based upon a first plurality of relative phases of a first plurality of transitions of the incoming bit stream; and

determining a subsequent average relative phase with respect to the reference clock signal based upon a second plurality of relative phases of a second plurality of transitions of the incoming bit stream and based upon the initial average relative phase.

4. The method of claim 3, wherein determining a sampling phase with respect to the reference clock signal comprises:

determining an initial sampling phase with respect to the reference clock signal based upon the initial average relative phase with respect to the reference clock signal; and

determining a subsequent sampling phase with respect to the reference clock signal based upon the subsequent average relative phase with respect to the reference clock signal.

5. The method of claim 4, wherein determining the initial sampling phase with respect to the reference clock signal is performed during a startup sequence of the incoming bit stream.

6. The method of claim 5, wherein determining the subsequent sampling phase with respect to the reference clock signal is also performed during the startup sequence of the incoming bit stream.

7. The method of claim 5, wherein determining the subsequent sampling phase with respect to the reference clock signal is performed during a data carrying portion of the incoming bit stream.

8. The method of claim 1, wherein determining an average relative phase of the detected transitions with respect to the reference clock signal further comprises normalizing a detected transition based upon its position with respect to the reference clock signal.

9. The method of claim 1, wherein the reference clock signal comprises a plurality of clock signal phases, each of which has a common frequency and each of which is offset in phase from each other of the plurality of clock signal phases.

10. The method of claim 1, wherein the reference clock has a frequency that is a multiple of a maximum transition rate of the incoming bit stream.

11. An apparatus for extracting bit values from an incoming bit stream, the apparatus comprising:

transition detection circuitry that receives the incoming bit stream and a reference clock signal, that detects transitions of the incoming bit stream with respect to the reference clock signal, and that determines relative phases of the transitions with respect to the reference clock signal;

transition phase averaging circuitry operably coupled to the transition detection circuitry that determines an average relative phase of the detected transitions with respect to the reference clock signal and that determines, based upon the average relative phase of the detected transitions with respect to the reference clock signal, a sampling phase with respect to the reference clock signal; and

bit stream sampling circuitry operably coupled to the transition phase averaging circuitry and to the transition detection circuitry that samples the incoming bit stream at the sampling phase with respect to the reference clock signal to extract the bit values.

12. The apparatus of claim 11, wherein the incoming bit stream complies with the Universal Serial Bus 2.0 interface standard.

13. The apparatus of claim 11, wherein in determining an average relative phase of the detected transitions with respect to the reference clock signal, the transition phase averaging circuit:

determines an initial average relative phase with respect to the reference clock signal based upon a first plurality of relative phases of a first plurality of transitions of the incoming bit stream; and

determines a subsequent average relative phase with respect to the reference clock signal based upon a second plurality of relative phases of a second plurality of transitions of the incoming bit stream and based upon the initial average relative phase.

14. The apparatus of claim 13, wherein in determining a sampling phase with respect to the reference clock signal, the transition phase averaging circuitry:

determines an initial sampling phase with respect to the reference clock signal based upon the initial average relative phase with respect to the reference clock signal; and

determines a subsequent sampling phase with respect to the reference clock signal based upon the subsequent average relative phase with respect to the reference clock signal.

15. The apparatus of claim 14, wherein the transition phase averaging circuitry determines the initial sampling phase with respect to the reference clock signal during a startup sequence of the incoming bit stream.

16. The apparatus of claim 15, wherein the transition phase averaging circuitry also determines the subsequent sampling phase with respect to the reference clock signal during the startup sequence of the incoming bit stream.

17. The apparatus of claim 15, wherein the transition phase averaging circuitry determines the subsequent sampling phase with respect to the reference clock signal during a data-carrying portion of the incoming bit stream.

18. The apparatus of claim 11, wherein in determining an average relative phase of the detected transitions with respect to the reference clock signal the transition phase averaging circuitry further normalizes a detected transition based upon its position with respect to the reference clock signal.

19. The apparatus of claim 11, wherein the reference clock signal comprises a plurality of clock signal phases, each of which has a common frequency and each of which is offset in phase from each other of the plurality of clock signal phases.

20. The apparatus of claim 11, wherein the reference clock has a frequency that is a multiple of a maximum transition rate of the incoming bit stream.

21. The apparatus of claim 11, wherein the transition detection circuitry comprises:

a plurality of flip-flops, each of which is operably coupled to receive the input bit stream as its data input and a respective phase of the reference clock signal as its clock input;

a first plurality of logic gates, each of which is operably coupled to receive a respective pair of flip-flop outputs as its inputs to detect a positive to negative transition of the input bit stream; and

a second plurality of logic gates, each of which is operably coupled to receive a respective pair of flip-flop outputs as its inputs to detect a negative to positive transition of the input bit stream.

22. An apparatus for extracting bit values from an incoming bit stream comprising:

means for detecting transitions of the incoming bit stream;

means for, for each transition of the incoming bit stream detected, determining a relative phase of the transition with respect to a reference clock signal;

means for determining an average relative phase of the detected transitions with respect to the reference clock signal;

means for, based upon the average relative phase of the transitions with respect to the reference clock signal, determining a sampling phase with respect to the reference clock signal; and

means for sampling the incoming bit stream at the sampling phase with respect to the reference clock signal to extract the bit values.